REMARKS

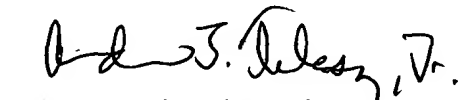
By this Preliminary Amendment, the specification has been revised to identify the parent application, and non-elected claims 1-12 have been canceled. Claims 13-20 are pending in this application. Entry of this Preliminary Amendment is respectfully requested.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

JONES VOLENTINE, LLC



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SEC.0467

FERROELECTRIC RANDOM ACCESS MEMORY DEVICE AND FABRICATION METHOD THEREFOR

This application claims priority under 35 U.S.C. §119 to Korean Application No. 97-82093, which is hereby incorporated by reference in its entirety.

CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Serial No. 09/198,324, filed November 24, 1998, which is hereby incorporated by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor memory device and a fabrication method therefor, and more particularly, to a ferroelectric random access memory (FRAM) device and a fabrication method therefor.

2. Description of the Related Art

A ferroelectric material has a ferroelectricity. The ferroelectricity is a physical property in which if an external voltage is applied to electric dipoles arranged in the ferroelectric material, a spontaneous polarization of the electric dipoles is generated. A remnant polarization of some constant level remains even after the external electric field is removed. When the remnant polarization of the ferroelectric material is used for storing data, the data can be stored without an external voltage. Also, application of a reverse external field causes polarization in the opposite direction.

the present invention, which operates by detecting a charge change in the ferroelectric capacitor.

A transistor including a gate 104 formed by interposing a gate insulating layer 102 on a semiconductor substrate 100, a source region 106 and a drain region 107, is formed. An interlayer insulating film 108, preferably composed of a material selected from phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), tetraethyl orthosilicate (TEOS) and undoped silicate glass (USG), is deposited on the entire surface of the substrate 100 in which the transistor is formed. A contact plug 110 formed in the interlayer insulating film is in contact with the source region 106 of the transistor. A lower electrode 112 is formed on the contact plug 110.

A dielectric layer D including a lower seed layer 114, a ferroelectric layer 116 and an upper seed layer 118 is deposited on the lower electrode 112. An upper electrode 120 is formed on the upper seed layer 118, to thus complete a ferroelectric capacitor.

The seed layers 114 and 118 formed above and below the ferroelectric layer 116 prevent an imprint phenomenon from being generated in a ferroelectric capacitor by making the characteristics of the upper and lower interfaces of the ferroelectric layer match. The upper and lower seed layers 114 and 118 of the ferroelectric layer 116 are preferably formed of a material having a low crystallization temperature. By crystallizing the upper and lower seed layers 114 and 118 prior to the ferroelectric layer 116 during a thermal treatment for crystallizing the ferroelectric layer 116 into a stable perovskite structure, the ferroelectric layer 116 is crystallized from the upper and lower faces toward

substrate 100 in a conventional manner. Subsequently, an insulating material, preferably selected from PSG, BPSG, TEOS and USG, is deposited on the entire surface of the resultant structure and planarized to form an interlayer insulating film 108. Next, the interlayer insulating film 108 is partly etched to form a contact hole exposing the source region 106 and the contact hole is filled with a conductive material, thereby forming a conductive plug 110 connecting a source of the transistor and a lower electrode of the capacitor.

Then, a material for forming the lower electrode of the capacitor is deposited on the resultant structure in which the conductive plug 112 is formed, and then patterned using a conventional photolithography to form a lower electrode 112 of the capacitor. Here, the lower electrode of the capacitor is preferably formed of a Pt-group metal such as Pt, Ir, Ru or Rh, a conductive oxide such as IrO_2, RuO_2, RhO_2 or $LaSrCoO_3$, or a dual layer of a Pt-group metal layer and a conductive oxide layer.

Referring to FIG. 6, a lower seed layer 114, a ferroelectric layer 116 and an upper seed layer 118 are sequentially formed on the entire surface of the resultant structure in which the lower electrode 112 is formed. After the layers including the upper seed layer 118 are formed, the resultant structure is thermally treated, thereby crystallizing a perovskite structure of the ferroelectric layer 116 and stabilizing the same.

Here, the lower seed layer 114 and the upper seed layer 118 are formed of a material which induces the ferroelectric layer 116 to be crystallized into a uniform and stable perovskite structure throughout the ferroelectric layer during a thermal treatment